Abstract

In performing address translation from a virtual address space to a physical address space, when the virtual address space is divided into an area (P0), which is subjected to the address translation by TLB, and areas (P1 and P2), which are fixedly mapped to the physical address without being subjected the address translation, future extension of the physical address become difficult. A data processor comprises an address translation unit ATU that receives virtual address output from the CPU and outputs a physical address; the ATU includes a first translation lookaside buffer UTLB, a second translation lookaside buffer DTLB, a control circuit TLB_CTL that selects one of a first and a second translation lookaside buffers and performs address translation in accordance with an area of an address space in the virtual address. Since it is adapted so that the areas (P1 and P2), which are conventionally mapped fixedly by hardware, are subjected to the address translation by the DTLB, it is possible to extend a size of the physical address space later without changing the hardware.